What is claimed is:

1. A dynamic random access memory (DRAM) cell structure (100) formed in a semiconductor substrate having a first conductivity type and having a self-aligned contact, the DRAM cell structure comprising:

source (120) and drain regions of a second conductivity type that is opposite to the first conductivity type formed in the semiconductor substrate in spaced-apart relationship to define a channel region therebetween;

a layer of gate dielectric material formed on a surface of the semiconductor substrate above the channel region and extending to partially overlap the source region (120) and the drain region;

a conductive gate (104/106) formed on the layer of gate dielectric material over the channel region;

a layer of first dielectric material (108) formed on the conductive gate (104/106) to define, in combination with the conductive gate, a stacked gate structure;

a dielectric sidewall spacer structure (110) formed on sidewalls of the stacked gate structure and such that at least a first portion of the sidewall spacer structure is formed on gate dielectric material that overlaps the drain region and at least a second portion of the sidewall spacer structure is formed on gate dielectric material that overlaps the source region (120);

a layer of second dielectric material (112) formed over the first dielectric material (108) and extending over the first portion of the sidewall spacer structure (110) and the drain region and the source region (120), the second dielectric material (112) having a contact trench (116) formed therein, the contact trench (116) having a first edge that is

at least partially aligned over the conductive gate (104/106) and is at least partially defined by the second portion of the sidewall spacer structure, and a second edge that is aligned over the source region (120), the contact trench (116) defining an exposed surface of the source region (120);

a conductive lower capacitor plate (114/118) formed at least partially over the second dielectric material (112) and to cover the first and second edges of the contact trench (116) and the exposed surface of the source region (120);

a layer of capacitor dielectric material (122) formed over the lower capacitor plate (114/118); and

a conductive upper capacitor plate (124) formed over the capacitor dielectric material (122).

2. A DRAM cell structure as in claim 1 wherein the first conductivity type is P-type and the second conductivity type is N-type.

3. A DRAM cell structure as in claim 1 wherein the gate dielectric materials comprises silicon dioxide.

4. A DRAM cell structure as in claim 1 wherein the conductive gate comprises a layer of first polysilicon having a layer of metal silicide formed thereon.

5. A DRAM cell structure as in claim 4 wherein both the lower capacitor plate and the upper capacitor plate comprise polysilicon.

6. A method of fabricating a dynamic random access memory (DRAM) structure (100) in a

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semiconductor substrate having a first conductivity type, the DRAM structure (100) including source (120) and drain regions of a second conductivity type that is opposite to the first conductivity type formed in the semiconductor substrate in spaced-apart relationship to define a channel region therebetween, a layer of gate dielectric material formed on a surface of the semiconductor substrate above the channel region and extending to at least partially overlap the source region (120) and the drain region, and a conductive gate (104/106) formed on the layer of gate dielectric material over the channel region, the method comprising:

forming a layer of first dielectric material (108) on the conductive gate (104/106) to define, in combination with the conductive gate, a stacked gate structure;

forming a dielectric sidewall spacer structure (110) on sidewalls of the stacked gate structure and such that at least a first portion of the sidewall spacer structure is formed on gate dielectric materials that overlaps the drain region and at least a second portion of the sidewall spacer structure is formed on gate dielectric material that overlaps the source region (120);

forming a layer of second dielectric material (112) over the first dielectric material (108) and extending over the drain region such that the second dielectric material (112) is separated from the drain region by gate dielectric material and the first portion of the sidewall spacer structure (110), and extending over the source region (120) such that the second dielectric material (112) is separated from the source region (120) by gate dielectric material

and the second portion of the sidewall spacer structure;

forming a contact trench (116) in the second dielectric material (120), the contact trench (116) having a first edge that is at least partially aligned over the conductive floating gate (104/106) and is at least partially defined by the second portion of the sidewall spacer structure, and a second edge that is aligned over the source region (120), the contact trench (116) defining an exposed surface of the source region (120);

forming a conductive lower capacitor plate (114/118) at least partially over the second dielectric material (112) and to cover the first and second edges of the contact trench (116) and the exposed surface of the source region (120);

forming a layer of capacitor dielectric material (122) over the lower capacitor plate (114/118); and

forming a conductive upper capacitor plate (124) over the capacitor dielectric material (122).

~~2~~ 1. A method as in claim ~~1~~ wherein the first conductivity type is P-type and the second conductivity type is N-type.

8. A method as in claim 1 wherein the conductive floating gate comprises a layer of first polysilicon having a layer of metal silicide formed thereon.

~~9~~ 4. A method as in claim ~~8~~ 3 wherein both the lower capacitor plate and the upper capacitor plate comprise polysilicon.